

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,166	01/18/2002	Hiroshi Horibe	50090-466	7602

7590

04/17/2003

McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

PAREKH, NITIN

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 04/17/2003

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/050,166

Applicant(s)

HORIBE, HIROSHI

Examiner

Nitin Parekh

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 February 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 and 12-20 is/are pending in the application.
- 4a) Of the above claim(s) 12-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3. 6) ☐ Other: _____

Art Unit: 2811

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I, claims 1-6 in Paper No. 7 is acknowledged.

Oath/Declaration

2. The oath/declaration filed on 01/18/02 is acceptable.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

Claims 1 and 2, lines 10 and 3 respectively cite: "...conductive parts on said chip...".

Therefore, the conductive parts on said chip must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

5. The Information Disclosure Statement filed on 01-18-02 has been considered.

Claim Rejections - 35 USC § 112

6. Claim 5 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5, lines 2-6 cite: "...the nearest bend to said inner lead among said plurality of bends of each bonding wire is located at a position at a distance from a limit on the side of the corresponding inner lead of a range extending over said chip toward the corresponding inner lead".

It is not clear from the description in the specification which distance applicant refers and what is the limit on the side of the inner lead.

It is also not clear which range extending toward the inner lead applicant refers.

Art Unit: 2811

Correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Shigeno et al. (US Pat. 6372625).

Regarding claim 1, Shigeno et al. disclose a semiconductor device comprising:

- a chip (11 in Fig. 2) provided with an insulating/passivating layer/part (not numerically referenced in Fig. 2; Col. 3, line 52) and a plurality of exposed bonding pads (12 in Fig. 2)
- a plurality of inner leads (15 in Fig. 2) arranged opposite/at a distance from the bonding pads
- a plurality of bonding wires (16 in Fig. 2) electrically connecting the bonding pads and the corresponding inner leads

- each of the bonding wires having a plurality of bends, the bends having a range of bending angles (23, 24, 25, etc. in Fig. 2; Col. 4, lines 40-50), being electrically isolated from conductive parts/pads on the chip and being arranged at an optional/desired positions on a surface of the chip, and
- the bonding wires being sealed in a resin (17 in Fig. 2) package providing the isolation/insulation for the bends from the conductive parts/pads of the chip

(Fig. 2 and 5; Col. 3, line 40- Col. 5, line 60).

Regarding claim 2, Shigeno et al. teach substantially the entire claimed structure as applied to claim 1, including the bends being electrically insulated from the conductive parts of the chip.

Regarding claim 4, Shigeno et al. teach substantially the entire claimed structure as applied to claim 1, and further teach the bonding wires being sealed such that one of the bends (see 23 in dotted line configuration in Fig. 2) is exposed on the surface of the resin package (Col. 4, line 62).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeno et al. (US Pat. 6372625) in view of Wark et al. (US Pat. 5847445).

Regarding claim 3, Shigeno et al. teach substantially the entire claimed structure as applied to claim 1, except at least one of the plurality of bends being in contact with the electrically insulating part so as to be insulated from the conductive parts of the chip.

Wark et al. teach using a device with a plurality of plurality of bonding wires having bends (62 in Fig. 3 and 4) where the bends (not numerically referenced in Fig. 3 and 4- see the bend at location 72 on the insulating part 70B and 70D respectively) are in contact with electrically insulating parts (70B and 70D in Fig. 3 and 4 respectively) so as to be insulated from the conductive parts/pads of the chip, to provide support and to minimize sagging for the bonding wires (Col. 5, line 40- Col. 6, line 63).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate at least one of the plurality of bends being in contact

Art Unit: 2811

with the electrically insulating part so as to be insulated from the conductive parts of the chip as taught by Wark et al. so that bonding wire support can be improved and the wire sagging can be reduced in Shigeno et al's device.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeno et al. (US Pat. 6372625) in view of Kumazawa et al. (US Pat. 5156323).

Regarding claim 6, Shigeno et al. teach substantially the entire claimed structure as applied to claim 1, except the bend nearest to the inner lead being at a level higher than that nearest to the chip.

Kumazawa et al. teach using bonding wires having a plurality of bends such that the bend (1a in Fig. 4) nearest to a bonding point on chip (A on chip 3 in Fig. 4) is at a higher level than the bend (1b in Fig. 4) nearest to a bonding point on a work piece/substrate (I in Fig. 4) to provide a protection against edge shorting and an increased wire loop length (Col. 4, line 1-25).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the bend nearest to the inner lead being at a level higher than that nearest to the chip as taught by Kumazawa et al. so that the edge shorting can be prevented and the length of the wire loop can be increased in Shigeno et al's device.

Art Unit: 2811

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

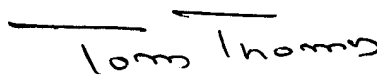
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
04-10-03


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800